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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,811	06/25/2007	Christian Pacha	V0195.0095	1611

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
12/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,811	PACHA ET AL.	
	Examiner	Art Unit	
	LONG NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-24 and 26-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-24 and 26-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2009* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in respond to applicant's amendment filed on 9/14/09.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the control unit/means (to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor) recited in claims 21 and 41-43 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 34-40 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Note that claim 34 fails to further limit the pulse generator of claim 30. Claims 35-40 are objected to because they depend on claim 34, and thus they have the same defect. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 21-24 and 26-43 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particularly, the specification does not discloses the pulse generator including "a control unit/means configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated" recited in the independent claims 21 and 41-43.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 21-23, 26-28, 30-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (USP 6,486,719).

With respect to claims 21-23, 26-28, 30-33 and 41-43, Figure 9 of Kim teaches a pulse generator (41d) for generating an input signal (SB, RB) to a flip-flop circuit (see Figure 4) from a clock signal (CLK) and from a data signal (D), which includes: a clock pulse field effect transistor (NA); a logic field effect transistor (NB); a first electrical reference potential (VSS), and a feedback transistor (N1) with the connections as recited in the claim. Clearly, Kim also teaches a control circuit (whichever circuit unit that is used to generated differential data signal D and DB) for generating differential data signals D and DB to control transistor NB and ND, respectively. Because the pulse generator in Figure 9 of Kim teaches the structure of the transistors (NA, NB and N1) are substantially identical to applicant's invention, so similar as applicant's invention, the pulses generator of Kim also meets the limitations "a control unit/means configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated" of claim 21. For claim 22, Figure 9 shows an additional clock pulse field effect transistor (P0) and a second electrical reference potential

(VDD). For claim 23, Figure 9 shows an additional feedback field effect transistor (P1). For claims 30-33, Figure 9 shows the clock pulse FET (NA), the logic FET (NB) and the feedback FET (N1) form a first signal path (in 411d), and wherein the pulse generator including a second signal path (in 412d) of additional transistors (NC, ND, and N3) which has the same circuit as the first signal path.

For claims 34-39, Figure 4 shows a circuit arrangement including a pulse generator (41, wherein the detail of 41 is shown in Figure 9 and is discussed in claims 21-23, 26-28 and 30-33 above), and a flip-flop (43). Note that the flip-flop circuit has storage FETs and switching FETs (i.e., the transistors that are used to form block 43 in Figure 4), wherein a first switching transistor would be the P-channel transistor (inside NAND gate 431) that has its gate receiving signal SB, and a second switching transistor would be the N-channel transistor (inside NAND gate 432) that has its gate receiving signal RB, a protective FET would be the N-channel transistor (inside NAND 431) that has its gate receiving signal SB.

For claim 40, the flip-flop (43) of Kim in Figure 4 includes complementary storage transistors configured to store a complementary storage signal which is complementary to the storage signal (see Figure 9).

Allowable Subject Matter

8. Claims 24 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if amended to overcome the rejections under 35 U.S.C. 112 above.

Response to Arguments

9. Applicant's arguments filed on 9/14/09 have been fully considered but they are not persuasive.

10. Applicant argues that "Figures 2, 4 and 5 are amended to include the control unit/means recited in claims 21 and 41-43. The control unit/means 250 is coupled to the gate terminal of the logic field effect transistor 207 and to the gate terminal of the logic field effect transistor 208". However, this does not overcome the drawings objections the rejection under 35 U.S.C. 112, 1st paragraph, since the control unit 250 (as applicant amended in the drawings) are merely a circuit for generating differential data signal D and /D. The control unit 250 that is used to generated data signal D and /D (as amended) is independent of the clock signal, and signals D and /D are for controlling transistors N3 and N4 (logic field effect transistor), while the clock pulse field effect transistor is controlled by the clock signal (i.e., clock pulse field effect transistor is not control by D or /D), so the disclosure does not disclose "a control unit/means configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated" recited in the independent claims 21 and 41-43.

Applicant also argues that "Kim does not disclose a control unit/means configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated". However, this argument is not persuasive because clearly, Kim also

teaches a control circuit (whichever circuit unit that is used to generated differential data signal D and DB) for generating differential data signals D and DB to control transistor NB and ND, respectively. Because the pulse generator in Figure 9 of Kim teaches the structure of the transistors (NA, NB and N1) are substantially identical to applicant's invention, so similar as applicant's invention, the pulses generator of Kim also meets the limitations "a control unit/means configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816